A 2–18-GHz Monolithic Distributed Amplifier Using Dual-Gate GaAs FET's

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Abstract—**This paper describes a 2–18-GHz monolithic distributed amplifier with over 6-dB gain, ±0.5-dB gain flatness, and less than 2.0:1 VSWR. Measured noise figure is below 7.5 dB, and power output capability is greater than 17 dBm. The amplifier is designed with dual-gate GaAs FET's instead of single-gate FET's for maximum gain over the design bandwidth. Cascaded amplifier performance will also be presented.**

I. Introduction

In THE PAST several years, distributed amplification [1] has enjoyed a renaissance due to the GaAs FET [2]–[4]. Applied originally to electron tubes, this amplification technique has the unique capability of adding device transconductance without adding device parasitic capacitance. This is accomplished by linking the parasitic shunt capacitance of the devices with series inductors to form an artificial low-pass transmission line. By terminating these links with resistive loads, the unwanted signals are dissipated while the desired signals are added in-phase at the output of the amplifier. The result is unprecedented gain-bandwidth product with flat gain and low VSWR. The structure is shown in Fig. 1.

II. Circuit Design

The topology of the 2–18-GHz distributed amplifier is shown in Fig. 2, and a SEM photograph appears in Fig. 3. In this design, there are essentially three features which distinguish it from previous distributed amplifiers. First and most important, the design uses dual-gate GaAs FET's in place of the more traditional single-gate devices. The contribution of dual-gate FET's to distributed amplification is equivalent to that of cascode-connected single-gate devices [5]. The dual-gate FET, which is in fact modeled as a cascode connection of single-gate FET's, has an input impedance comparable to single-gate devices but much higher isolation and output impedance. This is evident from the equivalent circuit models shown in Fig. 4, which were derived from measured *S*-parameters. (Note that the models include a common inductance of 0.04 nH to account for ground path inductance in the monolithic chip.) High reverse isolation in the device is necessary for high amplifier isolation and often extends the amplifier's bandwidth. High device output impedance, on the other hand, improves gain flatness and output VSWR, and increases gain. This is because the single-gate FET's output resistance is relatively low (250 Ω for a 250-μm device) and a significant load on the drain transmission line.

At low frequencies where the output resistances of the devices are virtually in parallel, a four-section design would result in a 62.5-Ω resistive load on the 50-Ω impedance transmission line. This problem is completely eliminated with the dual-gate (or cascode-connected) device.

The second feature of this design is the distribution of total gate width among the individual devices. In order to achieve a minimum gain of 7 dB with devices scaled from the model of Fig. 4 and 8-μm cm-wide transmission lines,

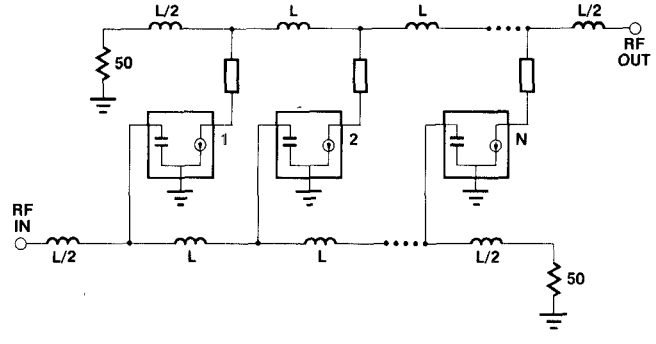

Fig. 1. Simplified distributed amplifier structure.

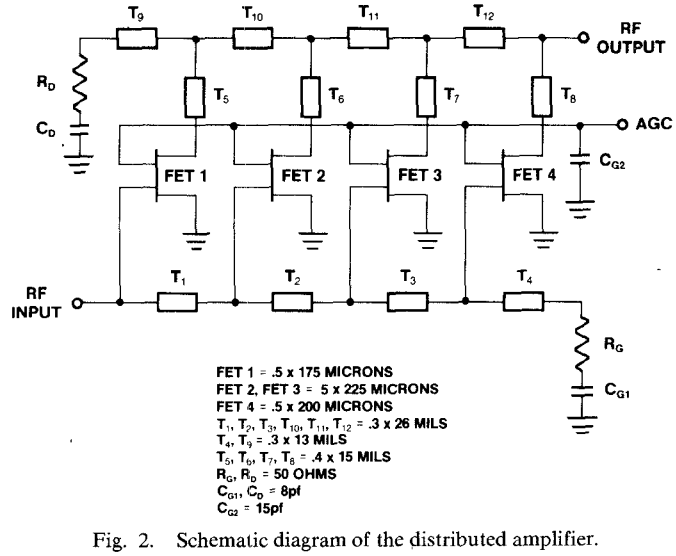

Fig. 2. Schematic diagram of the distributed amplifier.

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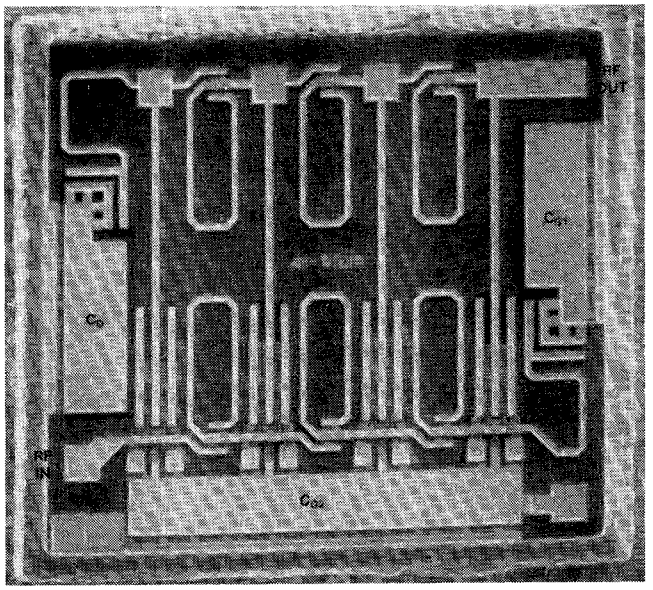

Fig. 3. SEM micrograph of the distributed amplifier.

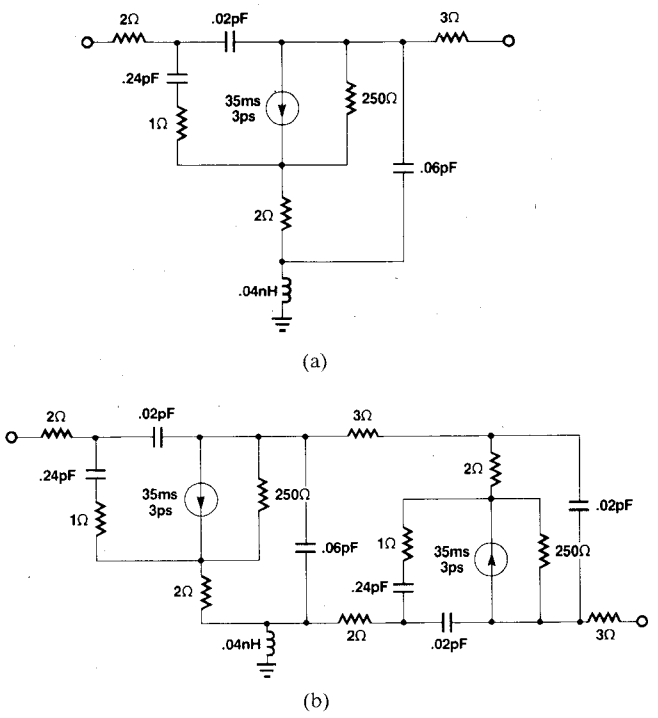

Fig. 4. (a) Single-gate and (b) dual-gate FET equivalent circuit models (250 μm).

which are fairly lossy, the amplifier requires at least 800 μm of gate width. This gate width could be theoretically partitioned into nearly any number of sections, but four sections prove optimal in many respects. First, it was desired to absorb the input and output bond wires into the distributed amplifiers input and output $L/2$ sections. For an input and output impedance of 50 Ω with 0.3-nH bond wires, this means

$$\sqrt{L/C} = 50 \text{ or } C = L/2500 = 0.3 \text{ nH}/1250 = 0.24 \text{ pF}.$$

This capacitance corresponds to a device gate width of 250 μm, but a choice of 200 μm leaves margin for error and the shunt capacitance of the high impedance transmission lines. Secondly, the four-section design offers a good compromise in gain flatness, VSWR, and noise figure over other 800-μm designs. This was determined by simulating the alternatives with a microwave analysis program. The four-section design is also more area efficient than its alternatives and results in a nearly square chip for ease of handling. As a final touch, the four individual device gate widths were optimized for VSWR and gain flatness. As shown in Fig. 2, the first and last sections are smaller than the two internal devices. This is primarily to absorb the parasitic capacitance of the input and output bonding pads.

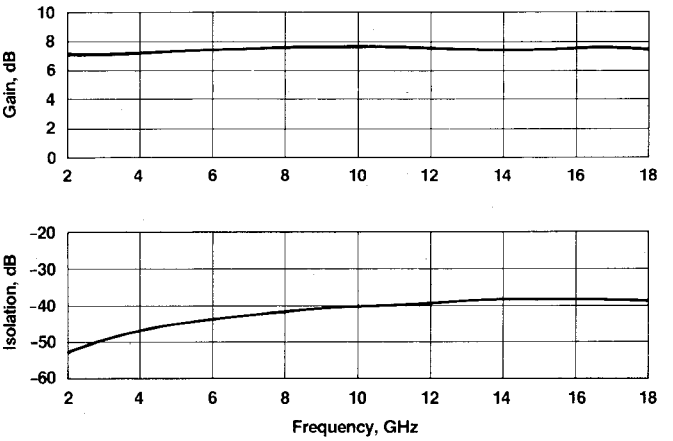

Fig. 5. Predicted gain and isolation of the dual-gate FET distributed amplifier.

The third feature of the design is its small area. At 0.75 mm × 0.85 mm the chip area is 0.64 mm^2, which yields a potential of over 2500 amplifiers per 2-in-diam wafer. This is chiefly a result of the single-turn inductors and wraparound ground. The single-turn inductor is modeled with lengths of coupled transmission line to account for coupling between the two major lengths and coupling to the FET sources (ground). If these inductors were laid out in a straight line rather than coiled one turn, the chip height would be unchanged at 0.75 mm but its length would be increased by 1.5 mm to 2.35 mm. The resulting layout would occupy nearly three times the area of the present one. The wraparound ground is also helpful in reducing chip area since the perimeter of the chip is normally not used. Via-hole grounds, on the other hand, require prime chip area and may be significant in size.

The amplifier contains three capacitors which are used for RF bypass to ground. CG1 and CD are used to bypass the input and output terminating resistors, respectively, so that dc power is not dissipated in these elements. The third capacitor, CG2, is used to bypass the second gates of the dual-gate FET's. This provides isolation from external dc circuitry and insures that the dual-gate FET operates as a cascode circuit. The FET sources are all grounded, thus requiring two bias voltages—one positive for the drain and one negative for the gate.

The simulated gain and isolation of the dual-gate distributed amplifier are shown in Fig. 5. From 2–18-GHz, the predicted gain is 7.25 ± 0.22 dB with greater than 35-dB isolation. Predicted return loss is shown in Fig. 6 and is

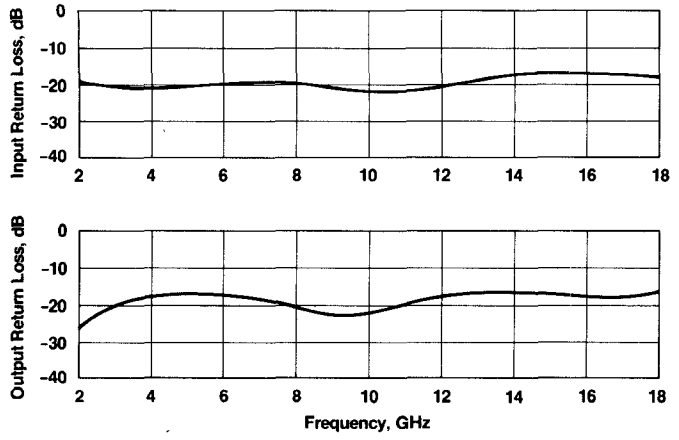

Fig. 6. Predicted input and output return loss of the dual-gate FET distributed amplifier.

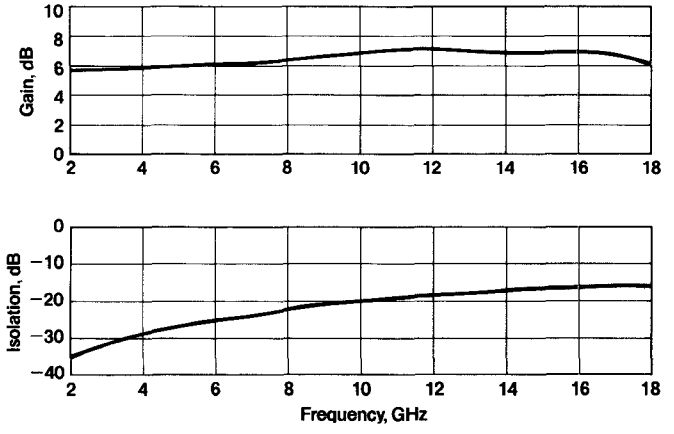

Fig. 7. Predicted gain and isolation of the single-gate FET distributed amplifier.

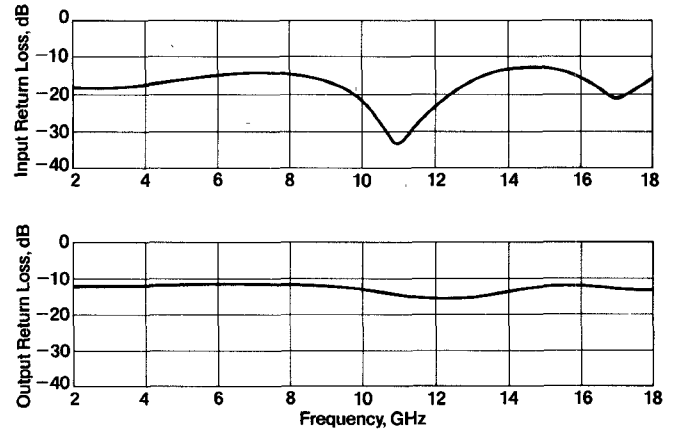

Fig. 8. Predicted input and output return loss of the single-gate FET distributed amplifier.

greater than 14 dB (1.5:1 VSWR) at both the input and output. Figs. 7 and 8 show the predicted performance of the same amplifier when the dual-gate FET models are replaced with the single-gate FET model from Fig. 4. It is clear that gain, gain flatness, isolation, output VSWR, and bandwidth are all degraded as expected. Noise figure, however, is lower in the single-gate design as shown in Fig. 9.

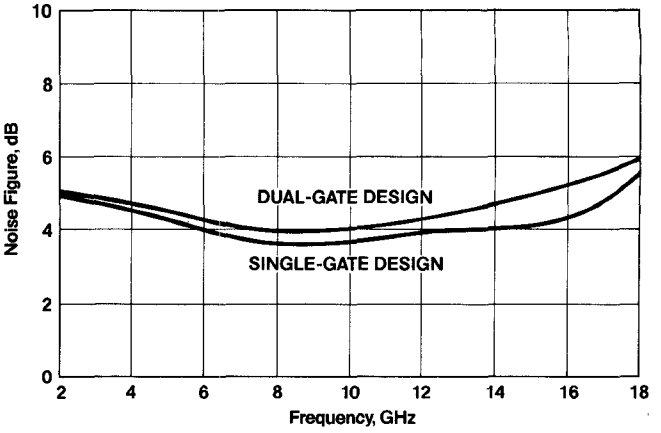

Fig. 9. Predicted noise figure of single-gate FET and dual-gate FET distributed amplifiers.

III. Circuit Fabrication

Ion-implanted GaAs is used as the starting material for the IC's due to its excellent uniformity and controllability. After implantation, the wafers are annealed at 800 °C until the active layer sheet resistance drops to approximately 500 Ω/square. This layer is then selectively etched to form mesas for the FET's and resistors. Later, the resistor mesas are trimmed to 800 Ω/square with a process that is controllable to a standard deviation of 15 percent.

The FET's in the IC are fabricated with the same process used for discrete FET's. The gates are formed on a nominally 0.5-μm-long base of TiW/Au, which is gold-plated to 0.7 μm. The resulting structure achieves very short gate length with large gate cross-sectional area for high device transconductance with low parasitic capacitance and resistance [6]. Source and drain ohmic contacts are formed with a AuGe/Ni/Au alloy.

Parallel-plate dielectric capacitors and surface passivation are provided by a thin layer of plasma-enhanced CVD silicon nitride. This process achieves a capacitance density of 390 pF/mm^2 with a standard deviation of less than 40 pF/mm^2.

Metallic interconnections are achieved with a two-level wiring process which provides surface connections, crossovers, and air bridges. The top level is situated 3 μm above the GaAs surface and is gold-plated to 1.5 μm. The bottom level rests directly on the semi-insulating substrate and is 0.8 μm thick. For additional thickness, the top level is deposited directly on the bottom level to achieve a thickness of 2.3 μm. These lines are designed for a dc current density not to exceed 5×10^5 amps/cm^2.

Wraparound ground technology is chosen over via-hole ground technology for low parasitic inductance and improved area efficiency. To form the wraparound ground, metal is first deposited and gold-plated to 2 μm on the frontside of the chips. The wafer is then lapped to 115 μm and backside metallized to complete the wraparound ground connection.

IV. Circuit Performance

Before backside-lapping and die-separation, the GaAs wafer is stepped and dc-probed for saturated current,

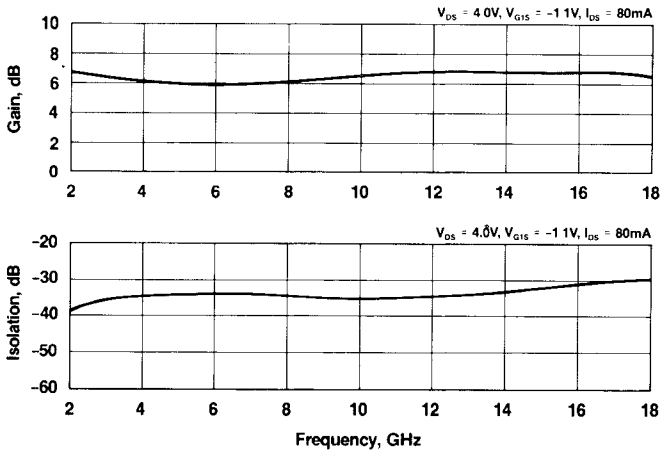

Fig. 10. Measured gain and isolation of the distributed amplifier

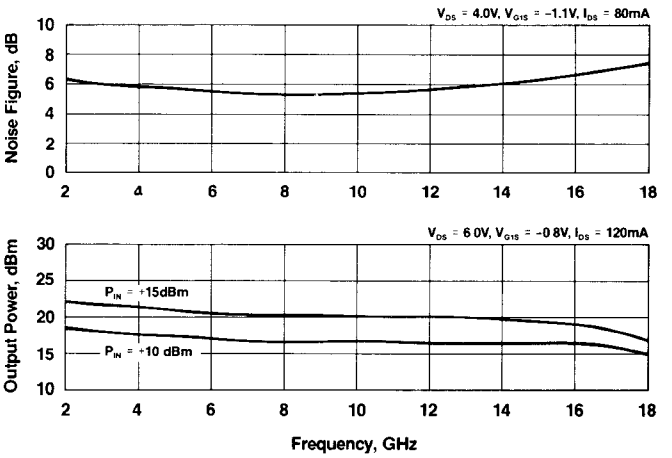

Fig. 12. Measured noise figure and output power of the distributed amplifier.

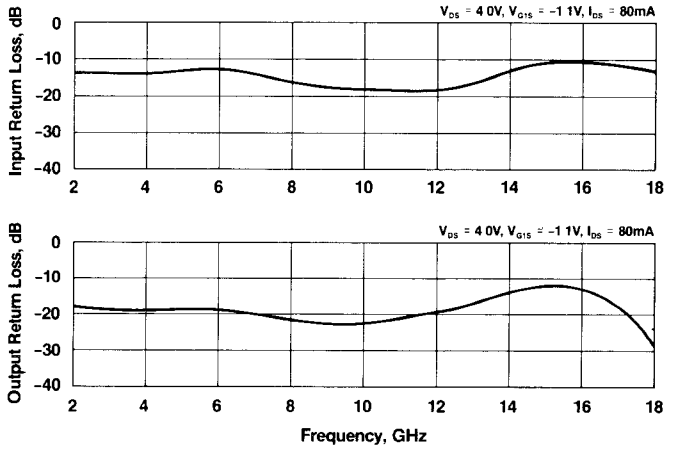

Fig. 11. Measured input and output return loss of the distributed amplifier.

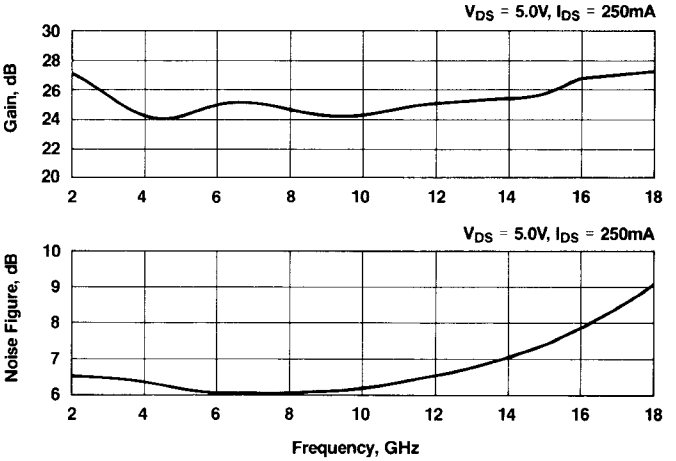

Fig. 13. Measured gain and noise figure of a four-stage distributed amplifier.

pinchoff voltage, and transconductance. Devices which are open-circuited, short-circuited, or otherwise fail the dc test are identified with an ink spot and later discarded. Data on passed devices is presented in summary form and may also be formatted into histograms for statistical analysis. The chips are then separated, visually inspected, and prepared for assembly into packages and thin-film hybrid circuits.

For RF evaluation, the amplifiers are mounted on 15-mil-thick alumina substrates. The substrate includes 50-Ω transmission lines, bias resistors, and plated through slots for ground. The data reported in this paper was measured on IC's mounted on the substrate with input and output bonding wires and no tuning. Bias was injected through external bias tee's.

Fig. 10 shows gain and isolation measured on a typical amplifier fabricated within process specifications. The gain is 6.3 dB $\pm$ 0.5 dB with greater than 25-dB isolation. Fig. 11 shows input and output return loss for the same chip. The worst case VSWR is 2.0:1 although it is less than 1.5 over most of the band. The device is biased at 4.0-V VDS, 80-mA IDS, which is half the saturated current level. Higher gain may be achieved with increased drain current, but gain flatness degrades slightly.

Noise and power performance are illustrated in Fig. 12. Noise figure is typically less than 6 dB and rises to 7.5 dB at 18 GHz. This can be reduced with an adjustment in bias but with a corresponding loss in associated gain. Output power is plotted from 2–18 GHz with constant input power levels of 10 dBm and 15 dBm. The device is capable of 20-dBm power over most of the band, but it degrades to 17 dBm at 18 GHz. Gain compression is more severe at the higher frequencies, as can be determined from the two plots.

Cascaded performance is demonstrated in Fig. 13. This data was measured on a four-stage amplifier consisting of two alumina substrates, four IC's, and ten bypass capacitors. The amplifier includes bias circuitry and measures only 5.1 mm $\times$ 12.7 mm $\times$ 0.38 mm (Fig. 14). This assembly shows that, even without integrating the blocking capacitors and bias circuitry on chip, a linear gain density of 50 dB per inch is easily achieved over the full 2–18-GHz band. With more compact hybrid layouts, this number could easily double.

The last figure (Fig. 15) illustrates a number of possible applications for the IC. As an AGC amplifier, gain variation is very flat over the full 2–18-GHz range when gate 2

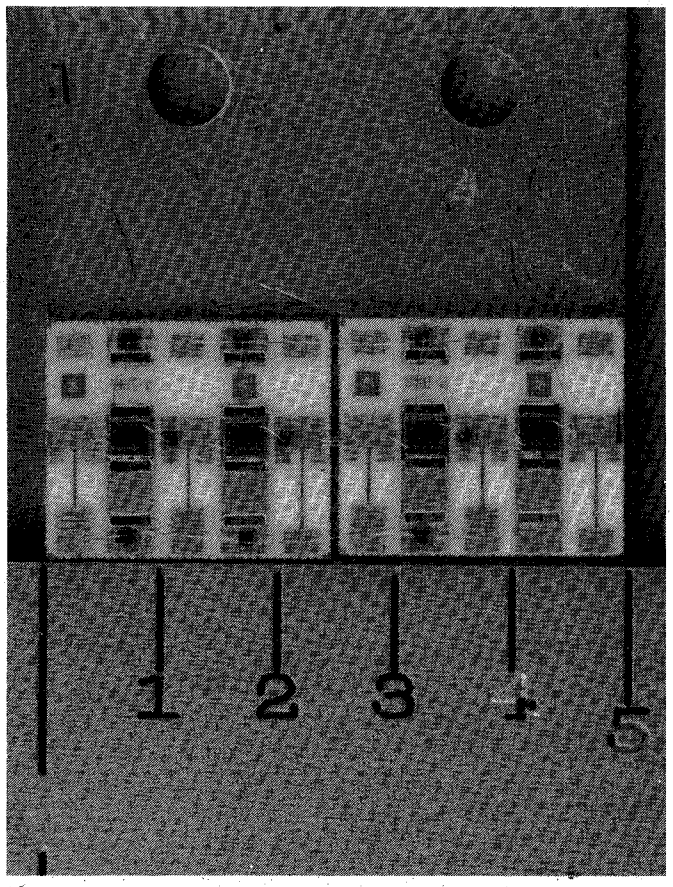

Fig. 14. Photograph of four-stage distributed amplifier.

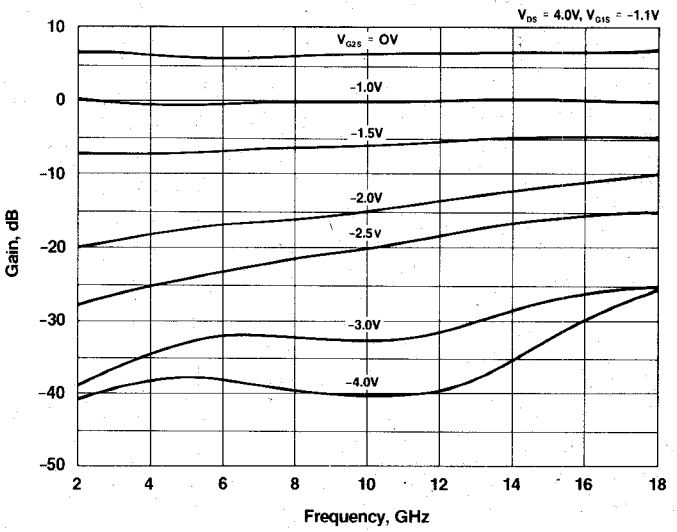

Fig. 15. Measured gain/loss as a function of gate 2 voltage.

voltage is varied between 0 V and −1 V. When the gate 2 voltage is made more negative, the amplifier becomes lossy and may be used as a limiter. Finally, when the voltage is increased to −4 V, the drain current drops to nearly zero and the amplifier provides over 25-dB isolation. This property could be used in switching applications since VSWR and reverse isolation remain less than 2:1 and greater than 25 dB, respectively, under all bias conditions.

V. Conclusion

A 2–18-GHz monolithic GaAs distributed amplifier with over 6-dB gain has been described. Dual-gate FET distributed amplifiers were compared to single-gate FET distributed amplifiers and were shown to provide more gain with better flatness, VSWR, and bandwidth. This is demonstrated in a four-stage amplifier which achieved 25.5-dB ± 1.5 dB gain from 2–18 GHz. The dual-gate FET distributed amplifier may also be used for many control functions by adjusting the gate 2 voltage.

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From 1978 to 1980, he was a Member of the Technical Staff at Hughes Aircraft, where he designed bipolar and GaAs FET microwave amplifiers in the range from 1 to 26.5 GHz. In 1980, he joined Avantek, Inc., as a Senior Engineer in the Device Evaluation Group, where he developed automated microwave test stations and a 22-GHz low-noise GaAs FET amplifier. He is currently a Member of the Technical Staff in the GaAs MMIC design group at Avantek, where he is responsible for developing a wide-band GaAs MMIC product line.

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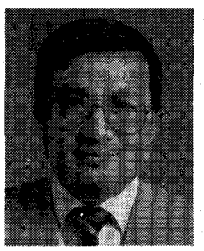
Thomas Andrade (M'80) photograph and biography not available at the time of publication.



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Dr. Huang is a member of Eta Kappa Nu.